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A b s t r a c t

A fast programmable processor on-line with a computer is being designed for the de-
tor MD-1. The processor reconstructs particle trajectories, classifies events and
cks whether selection criteria are satisfied. For an algorithm chosen the processor
ning speed is by a factor about 50 higher than that of the computer ES 1040. The pro-
sor will allow easy variation of selection criteria of the events during the experiment,
uce considerably the amount of data recorded in the computer memory and accelerate es-
tially the subsequent data processing.

n t e n t s

The magnetic detector MD-1 for experiments at the electron-positron storage ring
?-4 is under construction in the Institute of Nuclear Physics /1/. The detector mag-
(Fig.1) is a closed-type rectangular solenoid, its magnetic field being perpendicular
plane of beam orbits. Momentum measurement and reconstruction of particle trajecto-
are performed by 38 coordinate proportional chambers near the interaction region.
asic part of the chambers with a spacing of anode wires equal to 2 mm measures coor-
ates in the plane perpendicular to the magnetic field (X-Y-chambers). The chambers
uring a coordinate along the field direction (Z-chambers) have a 4 mm spacing. A sys-
of coordinate chambers contains 12 thousands of electronics channels. For particle de-
tion and identification shower-range and muon proportional chambers as well as gas
enkov and scintillation counters will be used.

The system will be triggered by pulses of fast "OR" of the proportional chambers in
coincidence circuit. This rather simple trigger must have a frequency not higher than
Hz. Events at such a triggering rate will enter a fast processor.

The fast digital processor will determine parameters of particle trajectories in an
t, classify the events, decide according to selection criteria whether the event must
recorded in the computer memory. Use of such a processor will allow flexible variation
election criteria during the experiment. With its help some reaction channels with
e cross section can be switched off (for example, $ee \to ee + ee$). Besides
use of information obtained by the processor will reduce the time for data process-
by the computer in the off-line mode.

Algorithm. After triggering information on the numbers of fired wires is transmitted
he processor that groups these numbers into tracks and determines their centres. The
k centres are transformed to the Cartesian coordinates. Further the processor operat-

es with coordinates of track centres. As the MD-1 magnetic field is homogeneous a particle trajectory is a helix.

Reconstruction of particle trajectories starts from the right (or left) half of the chambers with respect to the interaction region. The processor analyzes the events as follows. By looking through the points in X-Y-chambers four points lying on the same circle are found, a curvative radius and coordinates of its centre are determined. If such 4 points cannot be found calculation is performed by 3 points in X-Y-chambers. Then two points in Z-chambers are chosen and the helix is determined using these points and the circle above.

In most cases a particle trajectory intersects in addition chambers not used for trajectory reconstruction. These chambers are used to check if the trajectory found is real. The points from the trajectory are not considered further. Then the algorithm is repeated for the points remained.

For the real trajectory the processor determines if a particle came from the interaction region and such trajectories are continued to shower-range muon chambers and Čerenkov counters. Using this information the classification of events is performed by the processor. At the final step the processor checks whether or not the selection criteria are satisfied for the event and the events passed the criteria are recorded in the computer memory together with the results of processor analysis.

The algorithm of one helix reconstruction consists of 230 operations of summation, 190 comparisons, 100 multiplications, 20 divisions, 30 function calculations ($\sqrt{x}$, $\sin x$, $\cos x$, arc $\sin x$).

The number of point combinations which must be looked through to reconstruct an event depends on the number of particles in the event and on the way the points are chosen. Consider, for example, an event with 6 particles when each half of the system detects 3 particles, while looking through points starts from the end and middle chambers. For the most unfavourable choice of the points the algorithm of helix reconstruction must be repeated 28 times.

Choice of the variant of processor design. In our estimates use of the above algorithm at the Soviet or foreign computers takes some tens of milliseconds corresponding to the line capacity of tens of events per second only.

Three variants of the processor design have been considered:

1) hardware unit variant;

2) a processor with a built-in program;

3) a programmable processor.

The complicated algorithm practically excludes the first variant. The second one will lead to essential difficulties if the algorithm must be changed during the processor tuning and operation. We have succeded in finding the way to realize the third variant - construction of a programmable fast processor ($\sim$ 10 millions operations per second).

Processor structure. A processor arithmetic unit (AU) contains the hardware units (summers, multiplier, divider, comparison circuits) as well as permanent storages (PS) and working storages (WS) of different types. The AU units are joined by a unibus through which information can be transmitted from the output of any unit to an input of one or several other units. Instructions to exchange information or about operation modes of the units are given by the control unit (CU) through 40 parallel drive lines. Bits of the control word are distributed permanently among AU units. A number of drive lines necessary for unit operation is switched to each unit (Fig.2).

Processor operation. Instruction from CU to AU have a 30 nsec frequency. Each instruction has a position code for one operation. For example, the instruction shown in Fig.2 (second step of the program) rewrites a number from the divider output to the summer input. Each unit has input and output registers allowing, for example, after loading in the summer summands and instruction to sum or subtract to begin operation with other

nits. The instruction to extract information from the summer output will be given in a mber of CU steps with a total time greater than dead time of the summer.

The processor uses 24-bit floating-point numbers, 16 bits for mantissa, 6 - for pow-r, 2 - for power and mantissa signs. Numbers are normalized in the units before going o the unibus.

Unibus. The unibus consists of 24 drive lines, both ends of each line loaded on ave resistance. Integrated gates for input and output of information are located on the nibus printed plate near each unit, electrically between the connector contact and the nibus drive line to diminish the distributed capacity switched to the line. A cycle of nformation exchange at the unibus is 30 nsec. The unit locations are identical to each ther both by construction and electrical aspect allowing variation of the units and torages.

Hardware units. Memory. AU are based on the integrated series ECL with an average elay time of 3 nsec. Functions and time parameters of the units are presented in Table 1. he following units are included in AU:

1) Summer.

2) Multiplier. A conveyor multiplier is used. Data can be loaded with a 100 nsec ycle. The output register stores the first calculated products. After passing this num-er to the unibus the following product enters the register.

3) Divider.

4) Unit of function table values $\sqrt{x}$, $\sin x$, $\cos x$, $\arcsin x$. Range of each unction is divided into 64 intervals. PS stores function values corresponding to the in-erval ends. During the unit loading an argument is transmitted from the unibus, while he function indicator from the CU. The unit outputs subsequently three normalized numbers: unction values at interval ends and the difference between the argument and interval be-inning. The exact value of the function is calculated in the unibus using linear appro-imation with the help of the summer and multiplier. 1 μsec is spent on function calcul-tion *.

5) "Interval" unit. This unit is used to perform the operation often repeated in the lgorithm: whether or not a given number lies between two other numbers. Numbers are load-d subsequently. The result is transmitted to the mantissa sign line of the unibus.

6) Comparison circuit. Comparison of two numbers is also often repeated operation of he algorithm and as a rule preceeds to the transfer. The result of comparison is trans-itted to the mantissa sign line. The operation "leave the larger (smaller) number" is us-d while looking for the maximum (minimum) of the given set, the result being transmitted o the unibus after the end of search.

7,8) PS, WS and superfast storages. These units are used to store arrays of data, con-tants, intermediate results of calculations. A code of cell address or memory register oes from the CU drive lines.

9) "Stack" memory for 20 numbers. The unit is used for operation with arrays of un-nown length together with a unit "absence' of number".

10) "Absence of number" unit. The inputs are permanently switched to the unibus drive ines. During the enquest the unit transmits the information about presence of a number in he preceding CU step to the sign line.

Control unit. Control instructions changing the continuous sequence of calculations conditional or unconditional jumps , call to subroutine) are written in an array of he CU memory. All 40 drive lines are connected with a CU decoder . If such an instruction ppears CU stops instruction execution and jump to a new address is performed. Information bout the direction of the conditional jump is obtained by CU from the sign line of the nibus. CU can perform a jump according to the step counter if information about this was ecorded in previous control instructions.

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* To provide necessary accuracy arc sin x is tabulated near to $x = 1$ with the smaller step.

During algorithm programming some steps of the unibus may contain no operation. This situation occurs, for example, when one waits for the end of divider work. In this case a programmer can temporarily stop CU for some steps by writing a corresponding number in control instruction. If such an instruction appears, CU stops instruction ejecting and counting of CU cycles begins. When their number will be equal to a given one, CU continues ejecting program. Such a mode of operation allows essential saving of CU memory.

Processor speed. The processor considered is a specialized computer. Specialization consists in the special choice of hardware units as well as permanent algorithm of data input and preliminary data processing. At the same time this specialized computer is rather universal as required by possible algorithm changes. This is provided by total programmability as well as by the possibility to change AU units.

The higher speed as compared with fast universal computers is due to the following factors:

1. The hardware performance of all the units.
2. Processor structure allows simultaneous fulfilling of several operations. Two summers are included in AU to increase this factor.
3. Simultaneous transmission of data and instructions in several AU units is possible.
4. Processor architecture allows transmission of instructions from CU to AU at a speed $3 \cdot 10^7$ instructions per second.

To achieve the limiting speed the algorithm must be chosen so as to minimize the unibus standstills.

The estimate of algorithm fulfilling by the processor showed that 70 μsec are necessary to reconstruct one trajectory. The total time depends on the complexity of the event. For this problem the processor speed is about 50 times higher than that of EC-1040.

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Table 1. AU units and their time parameters

AU unit	CU instructions	Unit dead time, nsec	Time for data and instruction input, nsec	Time for result output, nsec
Summer	Input of the 1st, 2nd numbers. "+" or "-". Output of the sum.	300	60	30
Multiplier	Input of the 1st, 2nd numbers. Output of the product.	300	60	30
Divider	Input of dividend, divisor. Output of quotient.	1000	60	30
Table function values	Function type: $\sqrt{x}$, $\sin x$, $\cos x$, arc $\sin x$. Output of 3 numbers.	150	30	90
"Interval" unit	Input of the 1st, 2nd, 3rd numbers. Output of the result.	30	90	30
Comparison circuit	1st, 2nd number input. Operation type: comparison, comparison by absolute value, to leave smaller or greater. Output of the result	30	60	30
PS, WS (1 K)	Cell address $2^0 \div 2^9$. Number input. Number output	50*(PS) 200*(WS)	30	30
Superfast storage (8 registers)	Register address $2^0 \div 2^2$ Number input. Number output.	30	30	30
"Stack" memory	Number input. Number output. Reset.	30	30	30

* Use of PS and WS with such access times is planned.

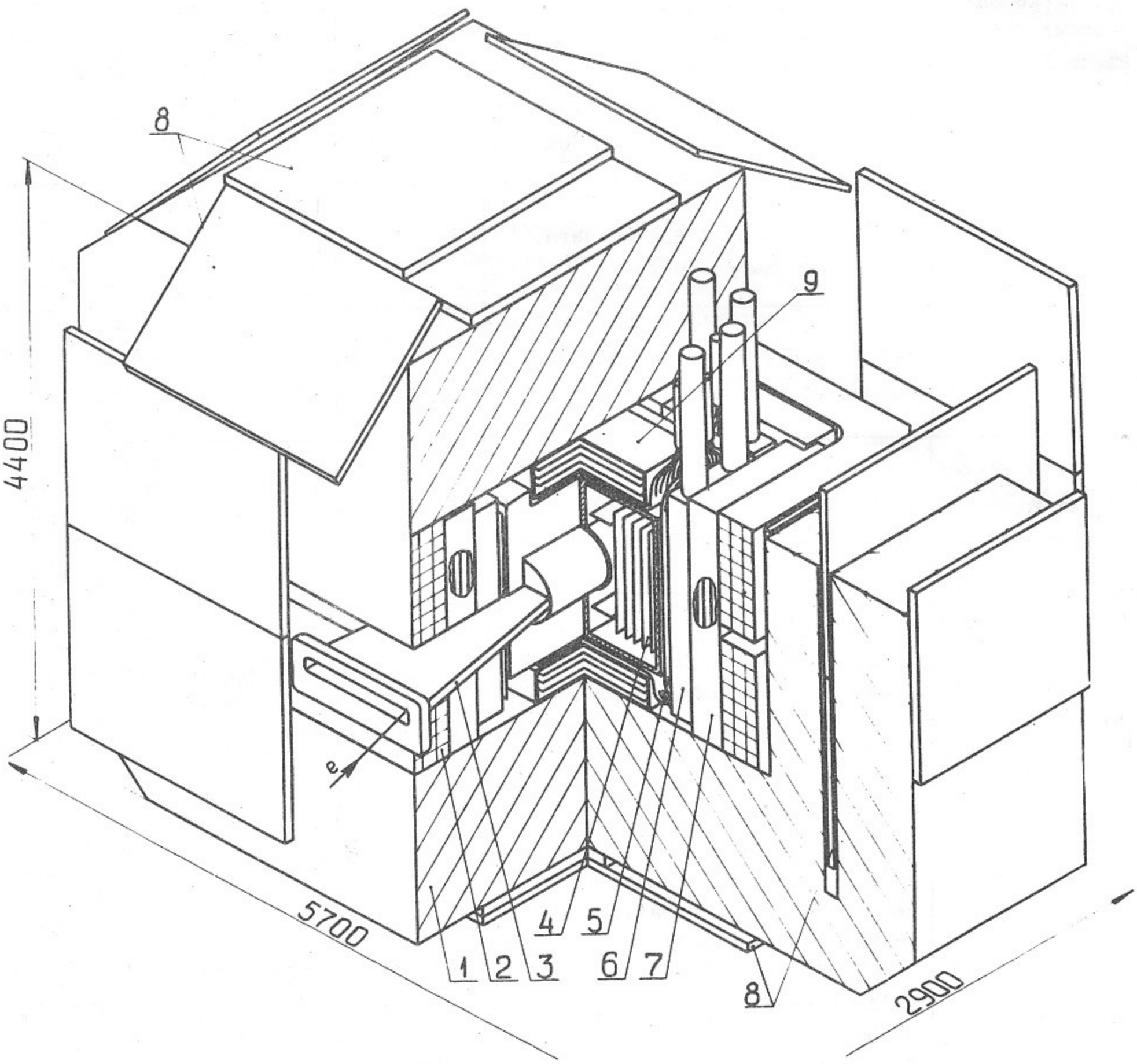

Fig.1 Magnetic detector MD-1. 1 - yoke, 2 - copper winding, 3 - vacuum chamber, 4 - coordinate chambers, 5 - scintillation counters, 6 - gas Čerenkov counter, 7,9 - shower-range chambers, 8 - muon chambers.

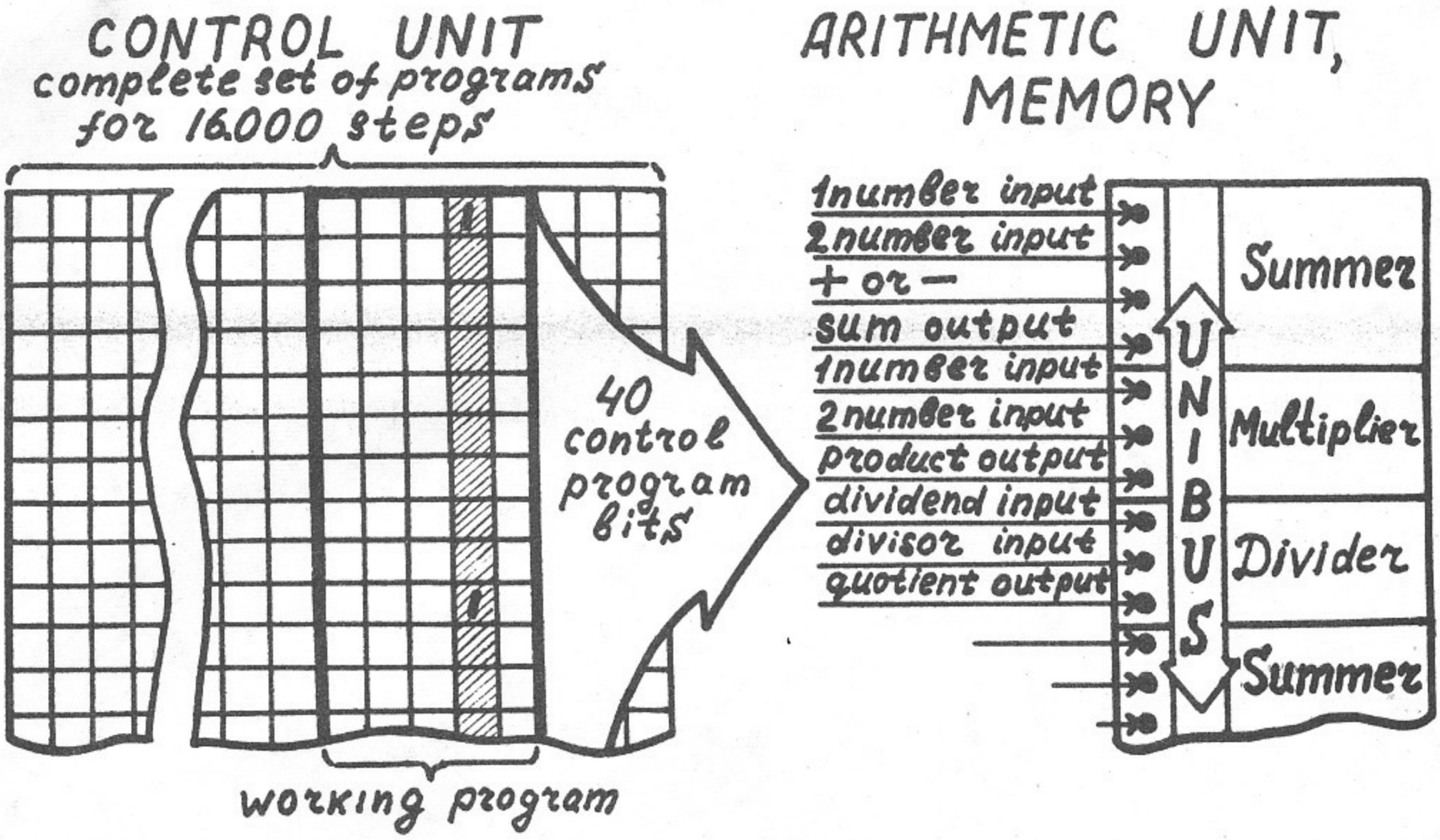

Fig.2 The principle of the processor operation.
The working program of 5 steps is marked out.
The dashed step corresponds to the transmission
of number from the divider output to the summer
input.

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